ABSTRACT OF THE DISCLOSURE

A variable current source model accurately determines timing delays for designs of circuits implemented in integrated circuits. A design for an integrated circuit specifies a resistive-capacitive ("RC") network. The RC network couples a driving point and a receiving point, and a circuit specified in the design, drives the RC network at the driving point. The variable current source model determines driving currents for the circuit at the driving point based on the RC network and a characterization model of the circuit. A timing delay between the driving point and the receiving point is determined by simulating the drive of the RC network with the driving current at the driving point.